ABSTRACT

[1116] An HDLC accelerator includes a deframer and framer to respectively accelerate the deframing and framing processes for PPP packets. The deframer includes an input interface unit, a detection unit, a conversion unit, and an output interface unit. The input interface unit receives a packet of data to be deframed. The detection unit evaluates each data byte to detect for special bytes (e.g., flag, escape, and invalid bytes). The conversion unit deframes the received data by removing flag and escape bytes, "un-escaping" the data byte following each escape byte, providing a header word for each flag byte, and checking each deframed packet based on a frame check sequence (FCS) value associated with the packet. The output interface unit provides deframed data and may further perform byte alignment in providing the deframed data. A state control unit provides control signals indicative of specific tasks to be performed for deframing.